G-line Manual: Control of DLI 99539 Current Amplifier with MC PCI-DIO24 digital I/O board

Author: D-M Smilgies 3/02
Purpose: spec macro to set the current amplification range by computer
Hardware: DL Instruments 99539 current amplifier
Measurement Computing PCI-DIO24 digital I/O PCI board
Custom-made cable D37-to-D37

Cable

<table>
<thead>
<tr>
<th>MC PCI-DIO24 function</th>
<th>pin #</th>
<th>DLI 99539 function</th>
<th>pin #</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>21</td>
<td>Digital Supply Return</td>
<td>28</td>
</tr>
<tr>
<td>C3</td>
<td>26</td>
<td>Remote/Local</td>
<td>6</td>
</tr>
<tr>
<td>C2</td>
<td>27</td>
<td>Gain Bit 3</td>
<td>25</td>
</tr>
<tr>
<td>C1</td>
<td>28</td>
<td>Gain Bit 2</td>
<td>5</td>
</tr>
<tr>
<td>C0</td>
<td>29</td>
<td>Gain Bit 1</td>
<td>24</td>
</tr>
<tr>
<td>A7</td>
<td>30</td>
<td>Gain Enable CH-8</td>
<td>4</td>
</tr>
<tr>
<td>A6</td>
<td>31</td>
<td>Gain Enable CH-7</td>
<td>23</td>
</tr>
<tr>
<td>A5</td>
<td>32</td>
<td>Gain Enable CH-6</td>
<td>3</td>
</tr>
<tr>
<td>A4</td>
<td>33</td>
<td>Gain Enable CH-5</td>
<td>22</td>
</tr>
<tr>
<td>A3</td>
<td>34</td>
<td>Gain Enable CH-4</td>
<td>2</td>
</tr>
<tr>
<td>A2</td>
<td>35</td>
<td>Gain Enable CH-3</td>
<td>21</td>
</tr>
<tr>
<td>A1</td>
<td>36</td>
<td>Gain Enable CH-2</td>
<td>1</td>
</tr>
<tr>
<td>A0</td>
<td>37</td>
<td>Gain Enable CH-1</td>
<td>20</td>
</tr>
</tbody>
</table>

Description: DIO24 and SPEC interface

- DIO24 has 3 banks A,B,C of 8 bits digital output each that produce +5V when HI, 0V when LO (TTL standard). A fourth bank D is reserved for configuring the board to either IN (read only) or OUT (read/write).
- The I/O register has to be configured in SPEC in the interface menu with the board addresses found in /proc/pci: the board addresses (BADDR) for R/W digital I/O are BADDR2, BADDR2+1, BADDR2+2, BADDR2+3, where BADDR2 ist the second address for the DIO24 in /proc/pci, e.g. if BADDR2=0xa800, the addresses for the R/W I/O are 0xa800, 0xa801, 0xa802, and 0xa803
- The “config” line in the interface menu reads
  IOPORT ADDR  <>MODE  NUM
  YES 0xa800  R/W 4
- The 4 in the NUM field means that four consecutive addresses are enabled.
  Note: the SPEC “port_put” and “port_get” functions will only work, if the addresses are declared in the interface configuration (SPEC safety feature)
- “gsetup” writes the addresses into the global variables
  RW_ADDR1 = 0xa800 (= BADDR2)
  RW_ADDR2 = 0xa801 (= BADDR2+1)
  RW_ADDR3 = 0xa802 (= BADDR2+2)
\[
\text{RW_ADDR4} = 0xa03 (= \text{BADDR2+3})
\]

If the BADDR is changed, both “config” and “gsetup” need to be updated.

- The DIO24 board needs to be configured as a first step. This is done by writing a specific code number to RW_ADDR4. The various codes are listed in page 9 of the PCI-DIO24 manual. Presently I have chosen code=128, i.e. all three register banks are configured as OUT. This is done in “gsetup”:
  
  \[
  \text{port\_put(RW\_ADDR4,128)}
  \]

Note: bank D/ RW_ADDR4 is write only and cannot be read back for error checking.

- Using `port\_put(address,value)` and `port\_get(address)` the R/W I/O can be written and read back, respectively; addresses are RW_ADDR1 through RW_ADDR3 corresponding to bank A through C, respectively; value can be any number between 0 and 255, and is interpreted bitwise for the eight outputs within each bank (A0 corresponds to 1, A1 to 2, …, A8 to 128, and so on)

- The spec macro “dliset.mac” defines the commands “dliset” and “dlishow”. “dliset” has as arguments the unit number (1 through 8 as well as 0 setting all units to the same value) and the gain (4 (corresponding to 1e4) through 10, 11=CAL, the calibration with a current source). “dlishow” keeps track of the various settings and displays them. “dlishow” has to be initiated with “dliset 0 4” at some point.

**Description: 99539**

- In order to write a number to a channel, the channel has to be enabled. This is done by setting Gain Enable CH-i to LO (i=1 to 8). If Gain Enable CH-i is HI, channel i is disabled (reverse logic). The Gain Enable bits are controlled by bank A/RW_ADDR1.

- The value to be set is given by Gain Bit 1-3 which are interpreted as an integer number GainBit1+2*GainBit2+4*GainBit3. If the number equals 0, the gain is 1e4, for 6 it is 1e10, for 7 it is CAL (calibration function of the 99539). The gain bits are controlled by bank C/RW_ADDR3.

- There are some timing issues on Gain Enable and Gain Bits. I found that I can get the board to work best, if I first write the gain bits, wait for 0.01sec, enable the unit to be set, wait for 0.01 sec and disable all units.

- The Remote/Local bit which should allow to set the range by computer, even if the channel is in local mode, is not working, as I expected – this problem needs fixing. Presently all Remote/Local switches on the front panel of the DLI 99539 have to be set to “Remote” for the computer interface to work.

- All features described have been implemented in SPEC macro “dliset.mac” which will be part of the user macro library (SPECD/umacros)